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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,179	09/15/2003	Gheorghe C. Cascaval	YOR920030127	9439

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MICHAEL J. BUCHENHORNER, ESQ
HOLLAND & KNIGHT
701 BRICKELL AVENUE
MIAMI, FL 33131

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,179	CASCAVAL ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-15 are presented for examination.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1- 15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons given below.

3. As to claim 1, no physical transformation can be found in the claim. No substantial practical application can be found in the claim. The practical application of the mechanisms for identifying the instructions that use the table and the for identifying the set of bits into instructions to index the indirection table is not clear.

4. As to claims 5, 10, no substantial practical application of the reading step and the identifying step and the creating step can be found in the claim. The computer program product is not tangible.

5. As to claims 2-4, claims 2-4 add no practical application to the parent claim. The plurality of register identified by register pattern could be just a list of register names or number on the table. The compatibility mode and extended mode are just logic values , or states , and achieved no practical application. Also, the practical application of the merging of the number of registers into the extended instruction is not clear.

6. As to claim 5, 10, no practical application can be found in reading the index field a, identifying an entry, and creating the extended instruction. No practical application of the extended instruction can be found .

7. As to claim 6,11, similarly, the no practical application can be found for the step of determining, extracting, and merging.

8. As to claims 7, 13, no practical application of the step of constructing the table, the generation of the instruction referencing entries , and the management of the table can be found in the claim. Similarly, the tale comprising the register specifies and 2B entries are not tangible. The computer program product is not tangible.

9. As to claims 8, 9, 14, the 2^B entries and the interpretation of register address fields in compatible mode are not tangible.

10. AS to claim 12, no substantial practical application can be found in merging the appropriate number of extended register specifies with eh instruction components.

11. AS to claim 15, interpreting an address field is an abstract idea.

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Devic (6,072,508).

13. As to claim 1, Devic taught at least :

a) an indirection table (see fig.3B 240) comprising a plurality of entries (64 entries) for encoding register patterns (offsets) , each register pattern identifying a register tuple (see starting address of multiple registers in register file 112,);

b) instructions for loading and storing entries in the indirection table (see fig.3A);

c) a mechanism for identifying instructions that use the indirection table (see the fetching of subsequent display list instructions in col.6, lines 37-47, see also col.7, lines 50-53); and

d) a mechanism for identifying a set of bits in instructions that are used to index into the indirection table (see partition bits 320 in fiog.3A, see col.8, lines 7-8).

14. As to claim 2, Devic taught a plurality of registers (see register file 112) identified by

a register pattern (see offset address as a starting partition in register file in col.7, lines 27-34, see also col.8, lines 45-53).

15. As to claim3, Devic taught compatible mode for interpreting register directly (see col.2, lines 18-43), and extended mode for interpreting the register access fields via the indirection table (see fig.3B 240).

16. As to claim 4, Devic also taught merging a number of registers (see partition bits 320 in fig.3A) into an expanded instruction (see instruction 210) that is used for remaining stages of instruction processing.

17. As to claim 5, 10, Devic taught :

a) reading index to an entry in an indirection table (see col.8, lines 7-8);

b) identifying an entry in the indirection table corresponding to the index (see index, col.8, lines 27,28) ,

wherein the entry comprises a plurality of register specifies (see register offsets) , and

c) creating an extended instruction comprising the plurality of register specifies (see partition bits in fig.3A) for processing of the instruction.

18. As to claims 6,11, 12, Devic also taught :.

a) determining whether to process the instruction is to be processed in an extended mode (see detection of the of next display list instructions requesting the parameter in col.6, lines 38-47);

b) extracting the index field of the instruction when the instruction is to be processed in extended mode (see col.8, lines 7-8); and

c) merging an appropriate number of extended register specifies (see the shift and increment the address counter to load the multiple registers in col.8, lines 38-50) with remaining components of the fetched instruction.

19. As to claims 7, 13, Devic taught :

a) constructing a table (see fig.3B 240), the table having a plurality of entries s and each entry specifying a combination of a plurality of registers (see the random registers of multiple registers in fig.3B);

b) generating an instruction referencing one of the entries in the table (see col.8, lines 7-8, see also fig.3A); and

c) managing the table by generating instructions to load table entries from memory and to store table entries to memory (see the loading of new addresses into the table in col.7, lines 15-22). , Devic showed the load into the table, but the store to a memory was not explicitly shown. However, examiner holds that Devic should be able implement store because Devic also taught a DRAM buffer for storing the frame data thought a bidirectional bus 118 (see fig.1, 118, col.6, lines 4-20)

20. As to claims 8, 14, Devic also included 2^B (see 64 entries = 2^6, see also the fig.2A 6 bits indexed into the table).

21. As to claims 9, 15, Devic also taught register address fields directly in a compatibility mode (see the loading at x and y locations by the Load instruction in col.2, lines 2-43).

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Gaither et al. (4,453,212) is cited for the teaching of index into a table with register pattern (see fig.1 and fig.2, col.3, lines 35-67, col.4, lines 1-5);

b) Tanahashi (4,466,056) is cited for the teaching of the index by the instruction bits into a table (see col.5, lines 65-68, col.6, lines 1-53);

c) Kaplinsky (4,361,868) is cited for the teaching of 2^B with the extended register specifiers (see fig.3, col.6, lines 27-68, col.7, lines 1-23) .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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